## REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action of April 21, 2008 (hereinafter "Office Action"). In response, Applicants have amended independent Claims 1, 10, 11, and 21 as indicated above to clarify that "nm comprises n multiplied by m" and that "y is less than nm", as discussed in further detail below. Also, new Claim 42 has been added, which recites that comparison result data from at least two different ones of the nm memory cell arrays are sequentially output "to a same one of the y data I/O pads." Support for this amendment can be found, for example, at Page 8, lines 18-24, and Fig. 4 of the present application. No new matter has been added.

Accordingly, Applicants respectfully request reconsideration of the pending claims for the reasons discussed below.

**The Section 112 Rejections**

Claims 1, 10, 11, and 21 stand rejected under 35 USC §112, second paragraph, as being indefinite. *See* Office Action, page 3. In particular, the Office Action asserts that the recitations of "*nm*-bit comparison result data" are unclear. *See* Office Action, Page 3.

In response, Applicants note that Claim 1 recites "*n* word lines" and "*m* column selecting lines". For example, in the embodiment illustrated in Figure 3 of the present application, the number of word lines $n = 2$, and the number of column selecting lines $m = 4$. As such, as correctly noted by the Examiner, the "*nm* memory cell arrays" and the "*nm* bit comparison data" of Claim 1 refers to the product or multiplication of the number of word lines *n* by the number of column selecting lines *m*. Thus, in the example embodiment of Figure 3, $nm = 8$, as illustrated by the 8 memory cell regions. As further discussed in the present specification:

> The comparator 16 compares, by 4 bits, test data [i.e., x-bit data] EDO1~4, EDO5~8, EDO9~12, EDO13~16, ODO1~4, ODO5~8, ODO9~12, and ODO13~16 output from **the memory cell regions (1) to (8)** [i.e., **nm memory cell arrays**], respectively, to generate **8-bit comparison result data** MA1 to MA8 [i.e., **nm-bit comparison data**] ...

Specification, Page 3, lines 18-21. In the interest of advancing prosecution, Applicants have amended Claims 1, 10, 11, and 21 to clarify that the nm-bit data and/or nm memory cell arrays recited therein "comprises *n* multiplied by *m*". No new matter has been added. Accordingly, Applicants respectfully request withdrawal of the rejections under 35 USC §112, second paragraph for at least these reasons.

**Independent Claims 1, 10, 11, and 21 Are Patentable Over the AAPA and Kim**

Independent Claims 1, 10, 11, and 21 stand rejected under 35 U.S.C. §103(a) as obvious over the alleged "Applicants' Admitted Prior Art" (AAPA[1]) in view of U.S. Patent No. 7,013,413 to Kim et al. (hereinafter "Kim"). Claim 1 as amended recites:

> 1. A method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected, wherein n, m, and x are integers greater than 1, wherein nm comprises n multiplied by m, and wherein y is less than nm, the method comprising:
>
> extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to each of the nm memory cell arrays in a test data write step; and
>
> comparing the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and **sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data** in response to a control signal **to the y data I/O pads, respectively**, in a test data read step. (*Emphasis added*).

Applicants respectfully submit that the combination of the AAPA and Kim fails to disclose or suggest at least the recitations of amended Claim 1 highlighted above. For example, the Office Action concedes that the AAPA fails to disclose or suggest sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data, but argues that Kim provides these recitations. *See* Office Action, Page 4.

Applicants respectfully disagree. As provided by the cited portion of Kim:

> **FIG. 4** shows part B (a dotted line part) in the data pass structure of **FIG. 3** in detail, that shows a pass that data from the core cell region

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1 For convenience, Applicants have adopted the term "Applicants' Admitted Prior Art (AAPA)" used in the Office Action. Use of this term is not an admission by Applicants that the material cited in the Office Action is prior art.

> 100 can be selectively outputted via the read data comparing part 500 to an output pad (DQ) during a normal operation or a DA mode test.
>
> Referring to **FIG. 4**, in a memory device according to an embodiment of the present invention, the read data comparing part **500** comprises a number of comparators **501-508** for receiving 8 bits data RD<0:7> read from the core cell region **100** according to a control signal (S_DATEST) when it is a DA mode test, compressing upper 4-bit data RD<0:3> and a lower 4-bit data RD<4:7> and generating a 1-bit data error<i>, 0<i<7, having information indicating whether a failure exists, multiplexers **509-512** for selecting the 8-bit data RD<0:7> read from the core cell region **100** when it is a normal mode or error <0:7> generated by the comparators **501-508** when it is a DA mode test according to the control signal (S_DATEST).

Kim, Col. 4, lines 50-67 (*emphasis added*). Accordingly, Kim discloses a circuit including comparators **501** to **508** that compare write data WD and read data RD to generate error signals error<0> to error<7>, respectively. As further illustrated in Figure 4 of Kim, the multiplexers **509-512** select between the 8-bit read data RD<0:7> (in normal mode) and the 8-bit error data error<0:7>(in test mode) for output in response to the control signal S_DATEST. *See* Kim, Fig. 4.

However, Applicants note that the cited portion of Kim discloses only "part B" in the overall data pass structure of Figure 3. Kim, Col. 4, lines 50-51. As further illustrated in Figure 3 of Kim, the data pass structure includes two sets of eight output pads DQA0-DQA7 and DQB0-DQB7. *See* Kim, Fig. 3. Indeed, Kim notes that "[d]ata transformed via shift registers **301-304** are...outputted serially via respective output pads (DQA0-DQA7 or DQB0-DQB7)." As further described in Kim:

> That is, since even data bits transferred via each shift register at an ascending edge of the clock signal TestClkR and odd data bits are transferred at a descending edge of the clock signal TestClkR, **8-bit data are transferred** serially in a packet form **via respective output pads** (DQA0-DQA7 or **DQB0-DQB7**)".

Kim, Col. 5, lines 24-29 (*emphasis added*). As such, while Kim may disclose serially outputting 8-bit data to 8 output pads, nowhere do the cited portions of Kim disclose or suggest selecting *nm*-bit comparison result data by *y*-bits for sequential output to *y* output pads, where *y* is less than *nm*. In other words, as the number of output pads disclosed in Kim

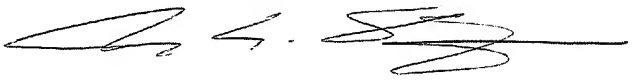
corresponds to the number of data bits, Kim does not disclose or suggest selecting the 8-bit data disclosed therein by less than 8 bits for sequential output to less than 8 output pads.

Accordingly, Applicants submit that neither the AAPA nor Kim discloses or suggests at least sequentially outputting y-bit comparison result data to y data I/O pads "by selecting, by y bits, the nm-bit comparison result data in response to a control signal", as recited by amended Claim 1. Thus, Applicants submit that amended Claim 1 is patentable over the combination of the AAPA and Kim for at least these reasons. Amended Claims 10, 11, and 12 include similar recitations, and are thus patentable for at least similar reasons. Also, dependent Claims 2, 3, 12, 13, and 37-42 are patentable at least per the patentability of Claims 1, 10, 11, and 21 from which they depend.

**Conclusion**

Accordingly, based on the remarks provided above, Applicants respectfully submit that all of the pending claims are now in condition for allowance. Thus, Applicants respectfully request withdrawal of the outstanding rejections, allowance of the pending claims, and passing the application to issue. Applicants encourage the Examiner to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,



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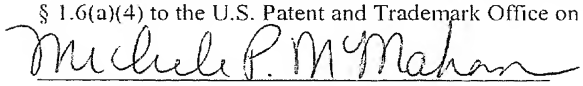

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